Claims:

1. A polishing pad useful for polishing a surface of a semiconductor substrate, the polishing pad comprising:
   (a) a polishing layer that includes:
      (i) a central region;
      (ii) an outer peripheral edge spaced from the central region; and
      (iii)a generally annular polishing region configured to polish the surface of a workpiece and having an inner periphery adjacent the central region and an outer periphery spaced from the inner periphery;
   (b) a first plurality of grooves in the polishing layer, each groove of the first plurality of grooves having a first end located within the central portion and a second end located within the polishing region; and
   (c) a second plurality of grooves in the polishing layer, each groove of the second plurality of grooves spaced from ones of the first plurality of grooves and having a first end located within the polishing region and a second end located in at least one of:
      (i) the outer peripheral edge; and
      (ii) radially outward from the outer periphery of the polishing region.

2. The polishing pad according to claim 1, wherein the second end of each groove in the first plurality of grooves is located proximate the outer periphery of the polishing region and the first end of each groove in the second plurality of grooves is located proximate the inner periphery of the polishing region.

3. The polishing pad according to claim 1, wherein ones of the first plurality of grooves are located alternatingly with ones of the second plurality of grooves.

4. The polishing pad according to claim 1, further comprising a third plurality of grooves in the polishing layer, each groove of the third plurality of grooves located entirely within the polishing region.

5. The polishing pad according to claim 1, further including a plurality of sets of branching grooves in the polishing layer, each groove in each set located entirely within the polishing region and having an end in fluid communication with a corresponding respective groove of the first plurality of grooves.

6. A method of chemical mechanical polishing a semiconductor substrate, comprising the steps of:
   (a) providing a polishing pad comprising:
      (i) a polishing layer that includes:
         (A) a central region;
         (B) an outer peripheral edge spaced from the central region; and
         (C) a generally annular polishing region configured to polish the surface of the semiconductor substrate and having an inner periphery adjacent the central region and an outer periphery spaced from the inner periphery;
      (ii) a first plurality of grooves in the polishing layer, each groove of the first plurality of grooves having a first end located within the central portion and a second end located within the polishing region; and
      (iii) a second plurality of grooves in the polishing layer, each groove of the second plurality of grooves spaced from ones of the first plurality of grooves and having a first end located within the polishing region and a second end located in at least one of the outer peripheral edge and located radially outward from the outer periphery of the polishing region; and
   (b) providing a polishing solution to the central portion of the polishing pad.

7. The method according to claim 6, further including the step of rotating the polishing pad while the semiconductor substrate is in contact with the polishing layer such that at least a portion of the polishing solution moves from ones of the first plurality of grooves to ones of the second plurality of grooves.

8. The method according to claim 6, further including the step of rotating the polishing pad while the semiconductor substrate is in contact with the polishing layer such that at least

a portion of the polishing solution moves from ones of the first plurality of grooves to corresponding immediately adjacent ones of the second plurality of grooves.

9. The method according to claim 6, further including the step of rotating the polishing pad while the semiconductor substrate is in contact with the polishing layer such that at least a portion of the polishing solution moves from ones of the first plurality of grooves to ones of a third plurality of grooves and from the third plurality of grooves to ones of the second plurality of grooves.

10. A polishing system for use with a polishing solution to polish a surface of a semiconductor substrate, comprising:
    (a) a polishing pad comprising:
        (i) a polishing layer that includes:
            (A) a central region;
            (B) an outer peripheral edge spaced from the central region; and
            (C) a generally annular polishing region configured to polish the surface of the semiconductor substrate and having an inner periphery adjacent the central region and an outer periphery spaced from the inner periphery;
        (ii) a first plurality of grooves in the polishing layer, each groove of the first plurality of grooves having a first end located within the central portion and a second end located within the polishing region; and
        (iii) a second plurality of grooves in the polishing layer, each groove of the second plurality of grooves spaced from ones of the first plurality of grooves and having a first end located within the polishing region and a second end located in at least one of the outer peripheral edge and located radially outward from the outer periphery of the polishing region; and
    (b) a polishing solution delivery system for delivering the polishing solution to the central portion of the polishing pad.